12 - MOSFETS! **Name:**____________________________ **Complete** ____

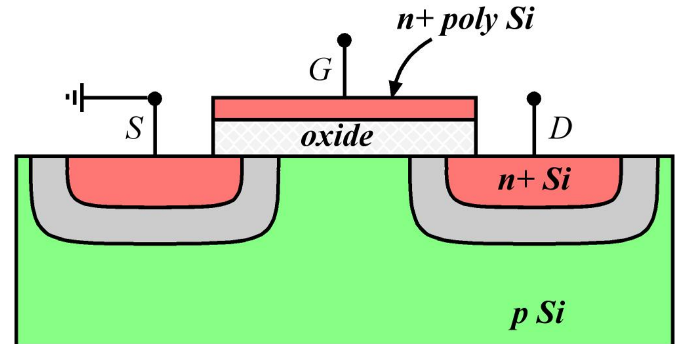
Agenda: (1) review the quiz / (2) 5 minutes minimum for lecture questions and review / (3) start the problems!

In-Class Problems

(1) The band diagrams and device cross-section for an NMOS device are shown below.

(a) for the **NMOS** device, if we add a positive drain voltage, and apply no gate voltage why can't we get current to flow from drain to source?

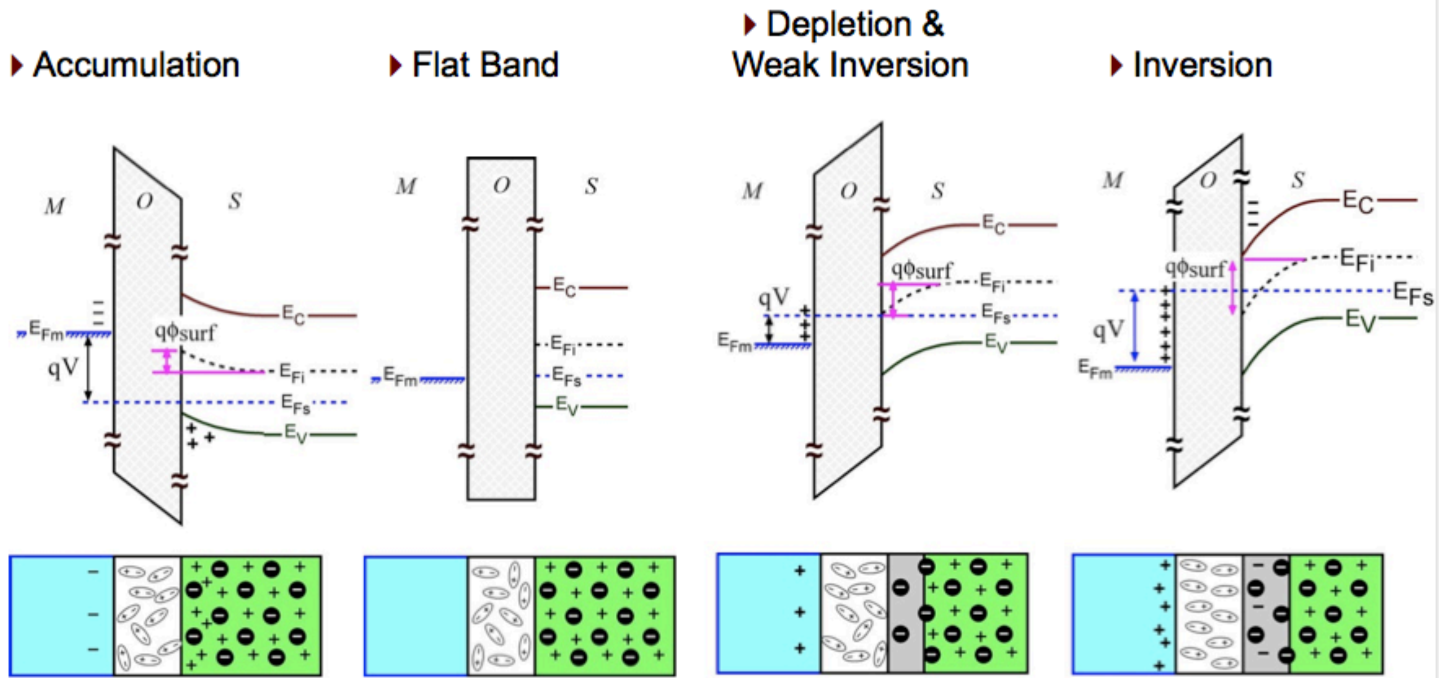
Back to back PN junctions (at least one is reverse biased).



(b) now, instead of just restating what you learned from the videos, lets test your basic understanding by having you redraw the diagrams below and at right for a **PMOS** device. Label them as 'inversion, accumulation, flat band, depletion' and… further label which one will be the most conductive and least conductive in terms of drain-to-source current.

(c) For this PMOS device, you would apply a negative voltage to the gate to turn it on. You know that if you keep increasing drain voltage you will run into saturation (like pinchoff), therefore, what is the polarity (+ or -) of the drain voltage you would apply to PMOS?

(d) lastly, for the 'depletion' diagram, draw a plot of E-field vs. distance for the metal, oxide, depleted semiconductor, and un-depleted semiconductor portions.



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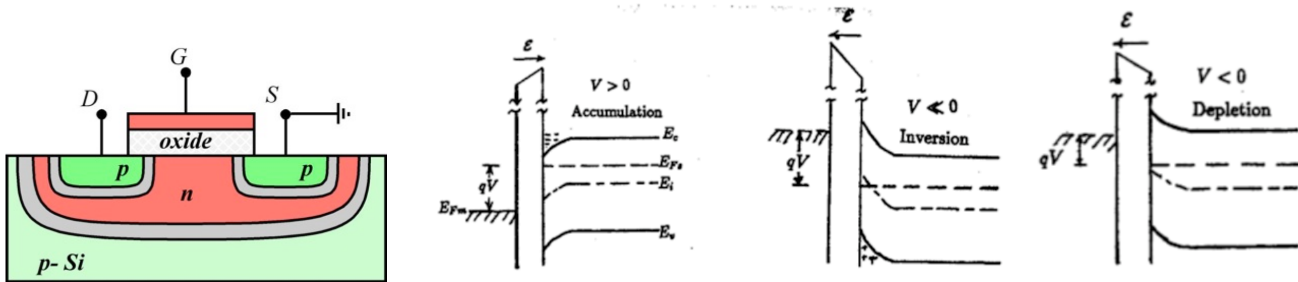
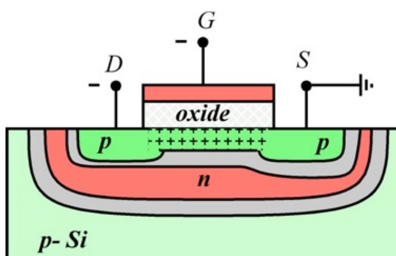
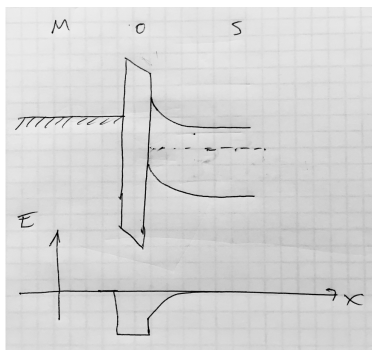
(b) The diagrams below are for PMOS fabricated on p-type substrate. You will see next lecture why we would do this. For today, you can simply make the substrate n-type and not have the extra PN junction and depletion region you see below.



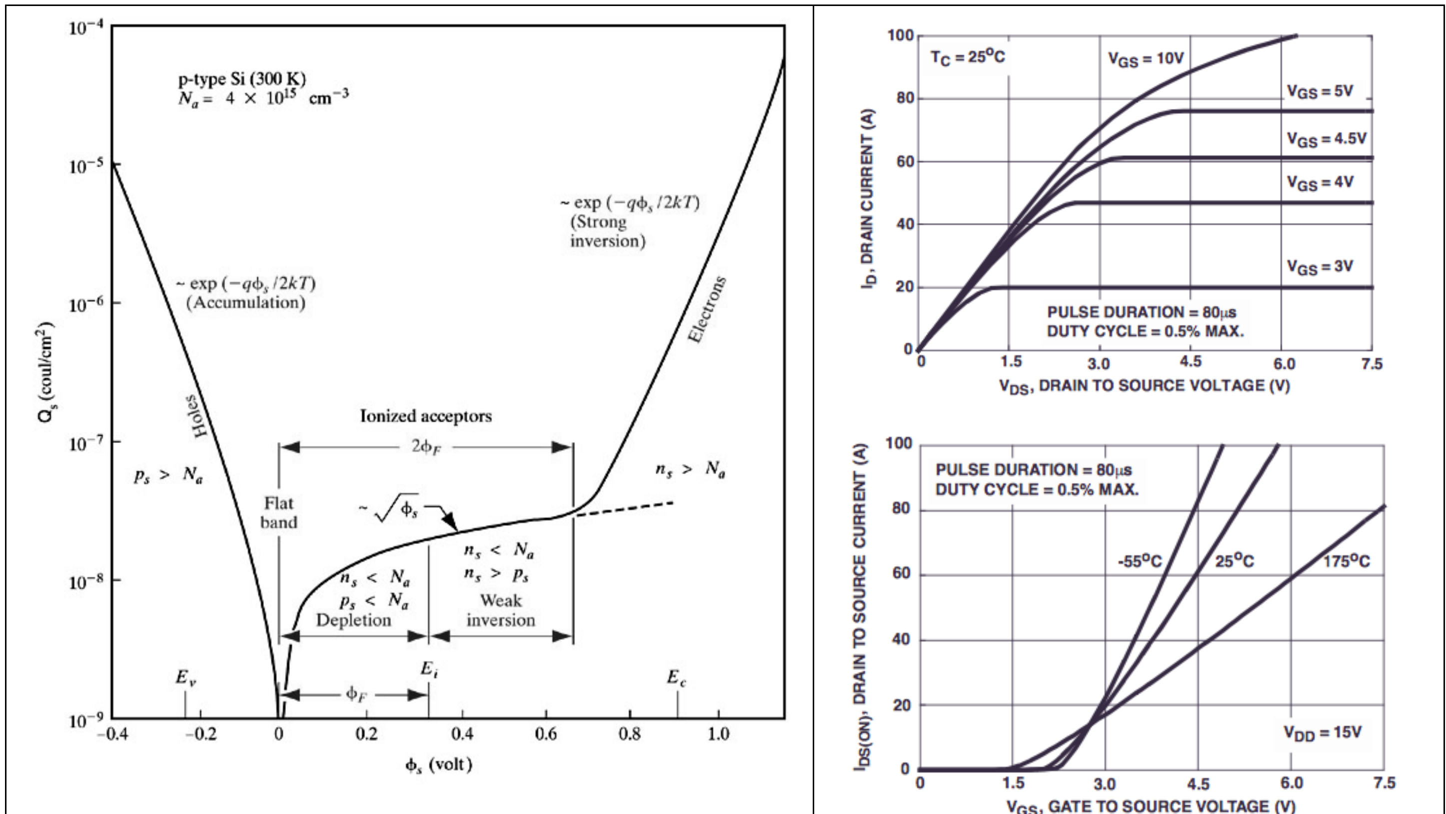
(c) negative to the drain (see image below). This makes sense if we are going to run into pinch-off, and next lecture will make even more sense when we make an inverter for the 1st time.



(d)



HINT: THIS GRAPH IS FOR SURFACE POTENTIAL (VOLTAGE <u>INSIDE</u> THE DEVICE, SEE IMAGE ON PREVIOUS PAGE)	HINT: THESE GRAPHS ARE FOR <u>EXTERNAL</u> VOLTAGE WHICH HAS TO COUPLE THROUGH A CAPACITOR TO CREATE INVERSION CHARGE. *Unrelated to the problem, you might notice that the results below are obviously for a power MOSFET…*



(2) Some multiple choice questions for NMOS. For the 1st few, remember that charge generation under the gate of a MOSFET follows either only depletion (dopant atoms) or Fermi-level shift type effects (carrier generation). Pick one answer for each. Do MORE than just look at the curves above, make sure you UNDERSTAND why as well!

(a) for accumulation, the charge increases with surface potential in a manner that is: linear / exponential / square root / quadratic.

(b) for depletion, the charge increases with surface potential in a manner that is: linear / exponential / square root / quadratic.

(c) for inversion, the charge increases with surface potential in a manner that is: linear / exponential / square root / quadratic.

(d) true or false, at threshold voltage you have already paid the maximum price (in terms of voltage) for depletion charge.

(e) true or false, if you increase substrate doping, you will have to shift the bands even more to get to threshold voltage

(f) true or false, the depletion region width maximizes at threshold voltage because you run out of dopant atoms to deplete

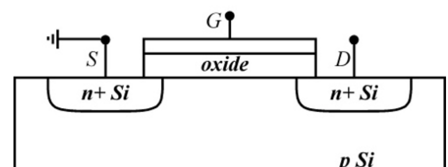
(g) true or false, at threshold voltage a square root function is taken over by an exponential function for charge generation

(h) true or false, inversion charge in the channel appears exponentially with external gate voltage (hint, Q=CV).

(3) Consider an ideal n-channel MOSFET on a p-Si substrate with the following characteristics (you may or may not need all the information provided below):

Na=10^{16}/cm^3
Oxide thickness = 50 nm
Area of gate = 1x1 μm

$\varepsilon_{Si}\varepsilon_0$ = 11.8 x 8.854x10^{-14} F/cm = 1.0x10^{-12} F/cm
$\varepsilon_{oxide}\varepsilon_0$ = 4 x 8.854x10^{-14} F/cm = 3.4x10^{-13} F/cm
ϕ_F = 0.347 eV



W_m= 300 nm

(a) Calculate the maximum charge per unit area that will appear under the gate.

(b) Calculate the gate capacitance per unit area.

(c) Calculate the threshold voltage for this device.

a) $W_m = 300$ nm (given) so $Q_d = -qN_aW_m = -47\ nC/cm^2$

$V_T = -\frac{Q_d}{C_i} + 2\phi_F$, need $C_i = \frac{\varepsilon}{d} = \frac{3.4\times10^{-13}\ F/cm}{50\times10^{-7}\ cm} = 68\ nF/cm^2$

so $V_T = \frac{47\ nC/cm^2}{68\ nF/cm^2} + 2\times0.347V = 0.691 + 0.694 = 1.385V$

(4) Some more EASY multiple choice questions for an ideal n-channel MOSFET device.

(a) If we apply positive voltage to the drain electrode, but zero voltage to the gate, we will not achieve any substantial flow of electrons from the source to drain, why?
___ because the channel will be depleted.
_X_ because we will always have at least one reverse biased pn-junction in the way.
___ magic.

(b) If we apply positive voltage to the drain electrode, and negative voltage to the gate, we would accumulate many holes underneath the gate oxide. This would increase the conductivity of the semiconductor under the gate oxide, but we will still not achieve any substantial flow of electrons from the source to drain, why?
___ because the channel will be depleted.
_X_ because we will still have at least one reverse biased pn-junction in the way.
___ ghosts.

(c) So now you realize how NOT to turn on an ideal n-channel MOSFET. Recall from the lecture notes that *for an n-channel MOSFET* we need to apply a positive voltage to gate that is greater than the threshold voltage (V_T) to allow flow of electrons from the source to drain. To allow current flow, what happens to the semiconductor near the gate oxide at the threshold voltage?
_X_ it inverts from p-type into n-type, then you have n-type (drain) / n-type (channel) / n-type (source) to allow flow!
___ the PN junction at the source or drain becomes forward biased.
___ Dancing with the Stars.

(d) So at threshold voltage and above, is there any depletion layer preventing electron flow from source, though the conducting n-channel and to the drain?
_X_ no, all regions that matter are n-type now!
___ yes – but it is so thin it does not matter.
___ more ghosts.

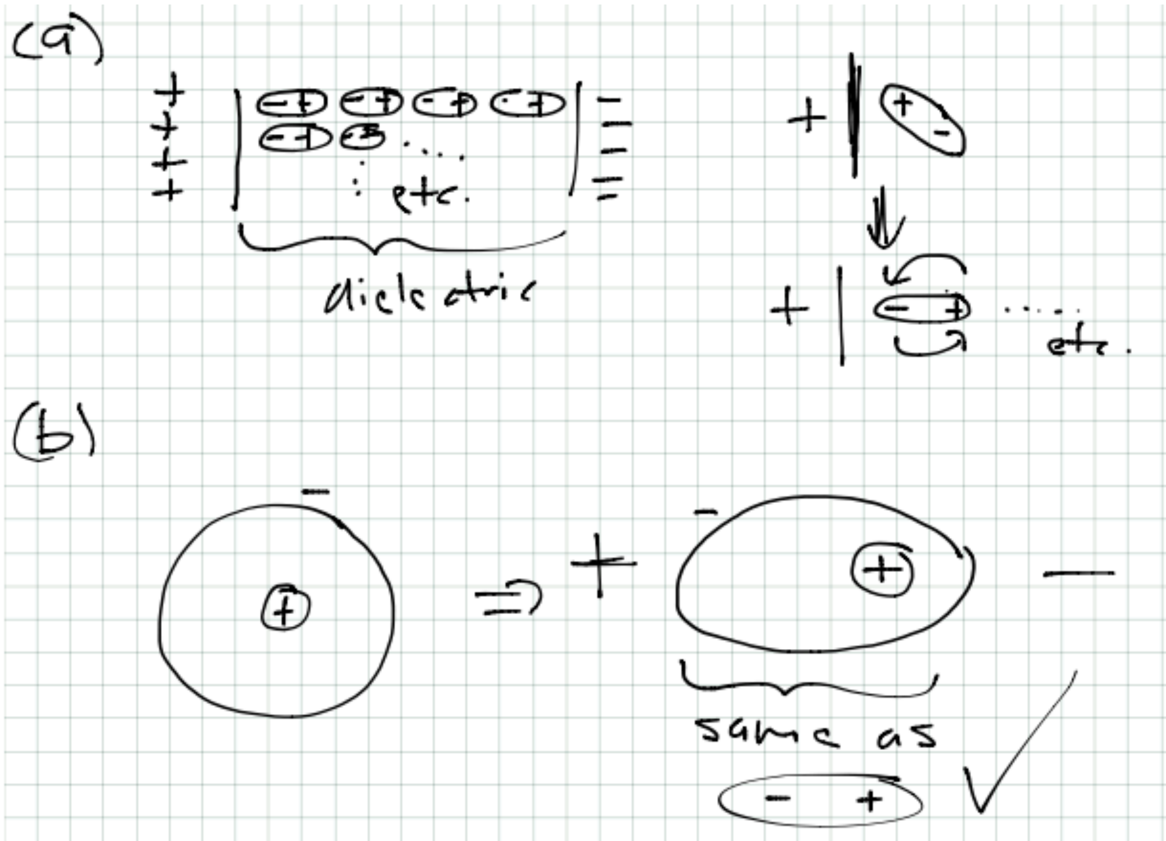
(5) Draw:

(a) a simple parallel plate capacitor diagram, and the dielectric material as having 'dipoles' in them like in our slides that can bend or rotate. Explain how charge is propagated through the dielectric and why a positive charge or voltage on one end leads to a negative charge or voltage on the other end….

(b) next draw an electron cloud or spherical electron orbital path around the nucleus of an atom (any simple atom, just draw it simple), keep the positive nucleus fixed in position and applied E-field. Does this create a dipole too? This shows

you that you don't need something to actually rotate, any insulating material can capactively propagate a charge through itself.

So you know…. materials that have higher permittivity (dielectric constant), simply allow more distortion of their electron clouds and/or in some cases have atomic bonds which can bend or rotate more to create dipoles….



(6) You create some crazy new transistor that is combination JEFT, MESFET, FET, and magical ghosts. The transistors DC drain current response is: $I_D = V_D(5V_G^2 + 1)$ Calculate the AC (small signal) transconductance for V_G=1V and V_D=1V.

Vg=1.0 V and Vd=1.0 V.

$$I_D = V_D(5V_G^2 + 1) \quad (A)$$

$$\frac{dI_D}{dV_G} = 0 + 10 V_D V_G = 10\ \Omega^{-1} = 10\ S$$